Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.063”**

**.041”**

**V-**

**V+**

**ZA589**

**MASK**

**REF**

**SUBSTRATE MUST BE BONDED TO V-**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential: V-**

**Mask Ref: ZA589**

**APPROVED BY: DK DIE SIZE .041” X .063” DATE: 9/13/17**

**MFG: ANALOG DEVICES THICKNESS .021” P/N: AD589**

**DG 10.1.2**

#### Rev B, 7/1